library ieee;

use ieee.std\_logic\_1164.all;

entity meio\_somador is port (

a : in std\_logic;

b : in std\_logic;

soma : out std\_logic;

carry : out std\_logic

);

end meio\_somador;

architecture arch\_meio\_somador of

meio\_somador is

begin

soma <= (a and not b) or (not a and b);

carry <= a and b;

end arch\_meio\_somador;